

IN THE CLAIMS

The current status of the claims is as follows:

1        1. (Original) For use in an integrated circuit of the type comprising at least two power  
2        supply domains in which each power supply domain comprises at least one module powered by the  
3        same voltage level, an apparatus for blocking an output signal in a first power supply domain from  
4        being sent to a second power supply domain when said second power supply domain is in a low  
5        power mode.

1        2. (Original) The apparatus as claimed in Claim 1 wherein said apparatus comprises:  
2              a power sense cell within said integrated circuit, said power sense cell capable of determining  
3              whether said second power supply domain is in a low power mode, and  
4              a logic circuit capable of blocking said output signal in said first power supply domain from  
5              being sent to said second power supply domain when said power sense cell determines that said  
6              second power supply domain is in a low power mode.

1           3. (Original) The apparatus as claimed in Claim 2 wherein said logic circuit comprises  
2       an AND gate having as a first input said output signal of said first power supply domain, and having  
3       as a second input a signal from said power sense cell.

1           4. (Original) The apparatus as claimed in Claim 2 wherein said power sense cell is  
2       located within said first power supply domain.

1           5. (Original) The apparatus as claimed in Claim 2 wherein said power sense cell  
2       comprises a Schmitt trigger circuit.

1           6. (Original) The apparatus as claimed in Claim 2 further comprising an apparatus for  
2       synchronizing blocked clock signals to prevent clock signals from being shortened by a signal from  
3       said power sense cell.

- 1        7. (Original) The apparatus as claimed in Claim 6 wherein said apparatus comprises:
- 2              a first D flip flop circuit having as one input a signal from said power sense cell, and having
- 3              as a second input a clock signal;
- 4              a second D flip flop circuit having as one input an output signal from said first D flip flop
- 5              circuit, and having as a second input said clock signal; and
- 6              an AND gate having as one input an output signal from said second D flip flop circuit, and
- 7              having as a second input said clock signal.

1           8. (Original) For use in an integrated circuit of the type comprising at least two power  
2       supply domains in which each power supply domain comprises at least one module powered by the  
3       same voltage level, an apparatus for blocking an output signal in a first power supply domain from  
4       being received in a second power supply domain when said first power supply domain is in a low  
5       power mode.

1           9. (Original) The apparatus as claimed in Claim 8 wherein said apparatus comprises:  
2        a power sense cell within said integrated circuit, said power sense cell capable of determining  
3       whether said first power supply domain is in a low power mode, and  
4        a logic circuit capable of blocking said output signal from said first power supply domain  
5       from being received in said second power supply domain when said power sense cell determines that  
6       said first power supply domain is in a low power mode.

1           10. (Original) The apparatus as claimed in Claim 9 wherein said logic circuit comprises  
2       an AND gate having as a first input said output signal from said first power supply domain, and  
3       having as a second input a signal from said power sense cell.

1           11. (Original) The apparatus as claimed in Claim 9 wherein said power sense cell is  
2       located within said second power supply domain.

1           12. (Original) The apparatus as claimed in Claim 9 wherein said power sense cell  
2       comprises a Schmitt trigger circuit.

1           13. (Original) The apparatus as claimed in Claim 9 further comprising an apparatus for  
2       synchronizing blocked clock signals to prevent clock signals from being shortened by a signal from  
3       said power sense cell.

- 1        14. (Original) The apparatus as claimed in Claim 13 wherein said apparatus comprises:
- 2              a first D flip flop circuit having as one input a signal from said power sense cell, and having
- 3              as a second input a clock signal;
- 4              a second D flip flop circuit having as one input an output signal from said first D flip flop
- 5              circuit, and having as a second input said clock signal; and
- 6              an AND gate having as one input an output signal from said second D flip flop circuit, and
- 7              having as a second input said clock signal.

1           15. (Original) For use in an integrated circuit of the type comprising at least two power  
2       supply domains in which each power supply domain comprises at least one module powered by the  
3       same voltage level, a method for blocking an output signal in a first power supply domain from being  
4       sent to a second power supply domain when said second power supply domain is in a low power  
5       mode, said method comprising the steps of:

6                 sensing with a power sense cell when said second power supply domain is in a low power  
7       mode; and

8                 blocking said output signal in said first power supply domain from being sent to said second  
9       power supply domain when said power sense cell determines that said second power supply domain  
10      is in a low power mode.

1           16. (Original) The method as claimed in Claim 15 wherein the step of blocking said  
2       output signal in said first power supply domain from being sent to said second power supply domain  
3       comprises the steps of:

4                 sending said output signal in said first power supply domain to a first input of an AND gate;  
5       and  
6                 sending a signal from said power sense cell to a second input of said AND gate.

1           17. (Original) The method as claimed in Claim 15 wherein said power sense cell is  
2 located in within said first power supply domain.

1           18. (Original) The method as claimed in Claim 15 wherein said power sense cell  
2 comprises a Schmitt trigger circuit.

1           19. (Original) The method as claimed in Claim 15 further comprising the step of:  
2           synchronizing blocked clock signals to prevent clock signals from being shortened by a signal  
3           from said power sense cell.

1           20. (Original) For use in an integrated circuit of the type comprising at least two power  
2           supply domains in which each power supply domain comprises at least one module powered by the  
3           same voltage level, a method for blocking an output signal in a first power supply domain from being  
4           received in a second power supply domain when said first power supply domain is in a low power  
5           mode, said method comprising the steps of:

6           sensing with a power sense cell when said first power supply domain is in a low power mode;  
7           and

8           blocking said output signal in said first power supply domain from being received in said  
9           second power supply domain when said power sense cell determines that said first power supply

1 domain is in a low power mode.

1           21. (Original) The method as claimed in Claim 20 wherein the step of blocking said  
2 output signal in said first power supply domain from being received in said second power supply  
3 domain comprises the steps of:

4           sending said output signal from said first power supply domain to a first input of an AND  
5 gate; and  
6           sending a signal from said power sense cell to a second input of said AND gate.

1           22. (Original) The method as claimed in Claim 20 wherein said power sense cell is  
2 located in within said second power supply domain.

1           23. (Original) The method as claimed in Claim 20 wherein said power sense cell  
2 comprises a Schmitt trigger circuit.

1           24. (Original) The method as claimed in Claim 20 further comprising the step of:  
2           synchronizing blocked clock signals to prevent clock signals from being shortened by a signal  
3 from said power sense cell.